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Final Report

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Summary:

The original research plan was to develop compliant substrate technologies for high In-containing InGaN growth. The progress in this research was unfortunately slowed by two factors. First, the PI could not find a close collaborator on InGaN growth and the PI's institute (then Cornell University) could not provide the infrastructure for the setup of the OMCVD reactor, which the PI received from Lucent Bell laboratory as a gift donation. As a result, no InGaN epitaxial growth experiment could be performed over the project period. Second, research results reported by other groups suggested that the proposed compliant substrate approach might not offer a solution to the problem of InGaN growth. The proposed approach was mainly based on the control and modification of the stress fields in the epitaxial layers. However, InGaN on sapphire, Si, or SiC is a far more complicated material system than traditional III-Von III-V or III-V on Si systems because the material quality is determined by many non-mechanical factors such as the surface chemistry, nucleation, and the built-in E-field, among other things. Therefore, we have made a few changes of our research directions, with the ultimate objective of advancing the knowledge and technology of "versatile substrates". The first change of research direction we made was to focus on the development of a working concept of versatile substrates. The goal is to establish a systematic, physics driven design methods for making composite substrates using materials that are readily available. The second change of research direction is to develop a truly viable material integration technology so that almost any two semiconductors can be bonded together without a joining layer, regardless of their crystal structures, mechanical and thermal properties. Furthermore, we like to assure that the technology is scalable to at least full 2" wafers. We believe that we have made significant progress in both areas.

Stress-engineered substrate:

We have developed an innovative concept and technology for stress-engineered substrates that can support very high-quality heteroepitaxial growth of materials of large lattice mismatch. For heteroepitaxial growth, dislocations are formed to relax the lattice mismatch. If the epitaxial material and the substrate have the same lattice structure (e.g., zinc blende), all threading dislocations in the heteroepitaxial layers are expected to share a common component in their Burgers vectors regardless of the detailed dislocation structures and propagation directions. That being said, all threading dislocations tend to behave similarly under certain external stress that

interacts most strongly with the common component of their Burgers vectors. Specifically, if the epitaxial layer has a larger lattice constant than the substrate **(positive mismatch)**, the threading dislocations in the epilayer tend to be bent towards the sides under **compressive stress**, terminating themselves at the edge of the sample or meeting another dislocation of compatible properties to form a dislocation loop. Similar behaviors will occur to negatively mismatched epitaxial material under tensile stress. Many buffer layer approaches including strain-graded buffer layers and strain-superlattice are using this mechanism to reduce the number of threading dislocations. However, all these buffer layer approaches have their limits. For the superlattice approach, the applied stress field is concentrated only in a very small (a few hundred Angstroms) region so dislocations may escape the superlattice region and thread up. For the strain-graded buffer layer approach, the stress field is inversely proportional to the thickness of the graded region so the stress diminishes as the thickness increases, giving dislocations chances to escape. Therefore, it requires a "long range" stress field that can interact effectively with the dislocations throughout the entire thickness of the epilayer. **In our approach, we use stress-engineering techniques to create substrates that can apply such stress field to dislocations.**

Because of the different thermal expansion coefficients between the substrate and the heteroepitaxial layer, thermal stress is generated when the sample temperature is different from the epitaxial growth temperature during annealing and cooling. The thermal stress is a "long range" stress that is uniform across the entire thickness of the epitaxial layer and the entire area of the sample except regions very close to the wafer edge. Therefore, if the sense (tension or compression) and the magnitude can be controlled properly, it would be an ideal source of stress to confine dislocations from threading up. One classical example is growth of GaAs on Si substrates. GaAs has a 4% larger lattice constant and a greater thermal expansion coefficient than Si. When GaAs layer is grown on Si and then annealed at a higher than the growth temperature, the compressive stress in GaAs due to thermal mismatch tends to confine dislocations from propagation and leads to an amazingly low (10^4 cm^{-2}) dislocation density. Although this result demonstrates the effectiveness of the thermal stress in dislocation confinement, it has little use in reality because the confined dislocations are "unleashed" during cooling when the thermal stress is switched from compression to tension. This problem is common to heteroepitaxial growth on any traditional substrates and can be solved using stress-engineered substrates. Stress-engineered substrates are made of multiple materials of different thermal expansion coefficients that are bonded together. The composite substrate can be engineered to have an effective thermal expansion coefficient that always provides stress in favor of dislocation confinement over the entire temperature range. The stress-engineered substrate may consist of two wafers of different thermal expansion coefficients bonded together by a thin joining layer for stress regulation. Let us consider the case that the epilayer is positively mismatched to the top portion of the substrate, which happens to have a larger thermal expansion coefficient than the epilayer. During annealing (above the growth temperature), the thin joining layer is softened so that the top portion of the substrate is essentially detached from the bottom portion and the epilayer will be under compressive stress in favor of dislocation confinement (for positive mismatch). However, during sample cooling, the thin joining layer is hardened significantly so that the top and bottom portion of the substrate is joined into one substrate. If the bottom portion of the substrate is so designed that the effective thermal expansion coefficient of the entire substrate structure is matched to or slightly lower than that of the epilayer, the epilayer will be stress free or in slight compression to avoid dislocation "unleash". Based on the same concept, many stress-engineered substrate structures can be designed using commercially available low cost substrates and each substrate design may be suitable for growth of a group of heteroepitaxial materials.

We have completed the following tasks towards the goal of establishing the scientific foundation, design principle, and fabrication technology for stress-engineered substrates for heteroepitaxial growth.

I. Establishement of detailed, quantitative models for dislocation confinement using stress-engineered substrates.

II. Demonstration of heteroepitaxial material with a reduced dislocation density using stress-engineered substrates.

III. Development of technology for synthesis of stress-engineered substrates.

IV. Develop a superior wafer bonding/fusion technology as the enabling technology of forming new and unique substrates.

V. Demonstrate device applications on innovative substrates.

Results:

We have demonstrated that in order to effectively confine the propagation of threading dislocations, dislocations need to interact with the right sense of stress and to obtain enough velocity. The velocity of dislocations depends on both stress and temperature, among other factors such as the detailed crystal and dislocation structures. Figure 1 shows the dependence of the stress and temperature for dislocations in some popular semiconductor materials.

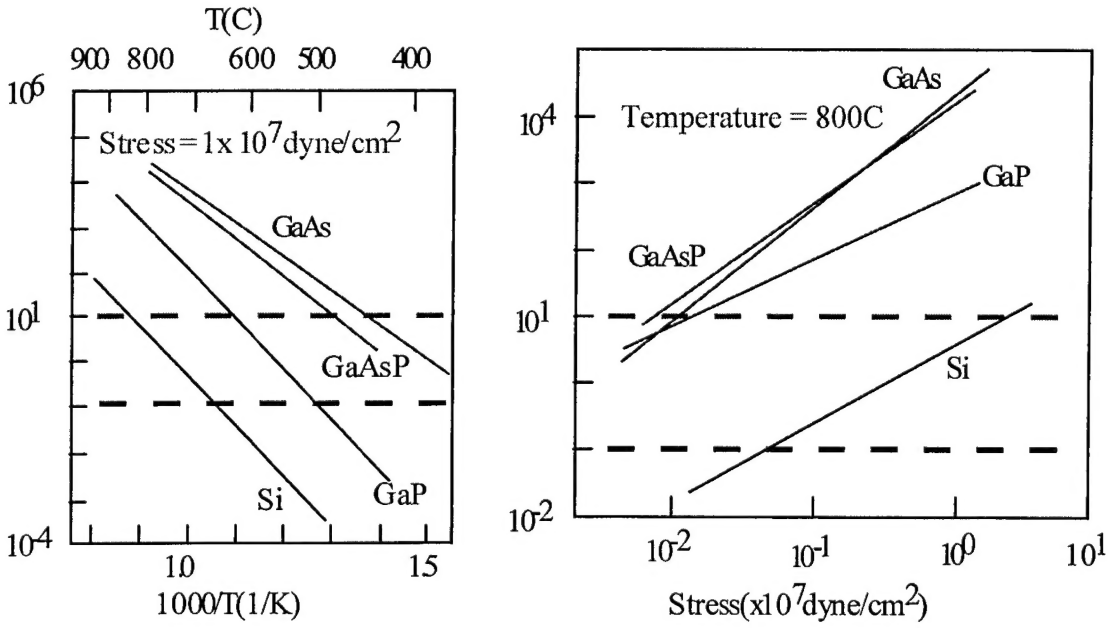


Figure 1. Dependence of dislocation velocity on temperature and stress for different semiconductor materials. The upper (red) dash line marks the points where dislocations move at a velocity of 10 μm/s and the lower (black) dash line marks the points where dislocations move at 0.1 μm/s. The former is believed to be the required speed for effective dislocation

confinement through bending and recombination; and the latter is what it might take for unleashing a confined dislocation when the sense of the stress is reversed (e.g. from compression to tension)

The data were derived based on the measurements of critical yield stress of bulk semiconductors in different applied stress and temperatures [2]. In Figure 1 the upper (red) dash line marks the points where dislocations move at a velocity of 10 μm/s and the lower (black) dash line marks the points where dislocations move at 0.1 μm/s. A speed of 10 μm/s is believed to be required for effective dislocation confinement through bending and recombination; and a speed of 0.1 μm/s is what it might take for unleashing a confined dislocation when the sense of the stress is reversed (e.g. from compression to tension). The large difference in required dislocation velocity for dislocation confinement and unleashing can be explained by the required dislocation travel distance for each process over a given time period. For confinement, a dislocation has to travel either to the edge of the sample or to meet another dislocation of comparable characteristics to form a loop. The lesser number of dislocations left in the material, the longer distance or higher speed they have to travel. That is how the well-known 1/h law was derived in reduction of dislocation density with increasing buffer layer thickness. On the other hand, a confined dislocation can thread up through "reverse bending" or "loop expansion" to the surface of the epilayer by a movement of only a few micrometers. That is why the required speed for unleashing a confined dislocation is much lower. It is worth mentioning that the data in Figure 1 are only for reference. The actual speed of dislocations can be affected significantly by many factors such as material hardening and dislocation pinning. When impurities are introduced to the material, material may be hardened so the speed of dislocation is reduced. Similar effects can also be caused by dislocation pinning particularly in a crosshatched configuration. Nonetheless, the data in Fig. 1 provide very useful information in design and analysis of heteroepitaxial growth and substrate effects, as to be shown next.

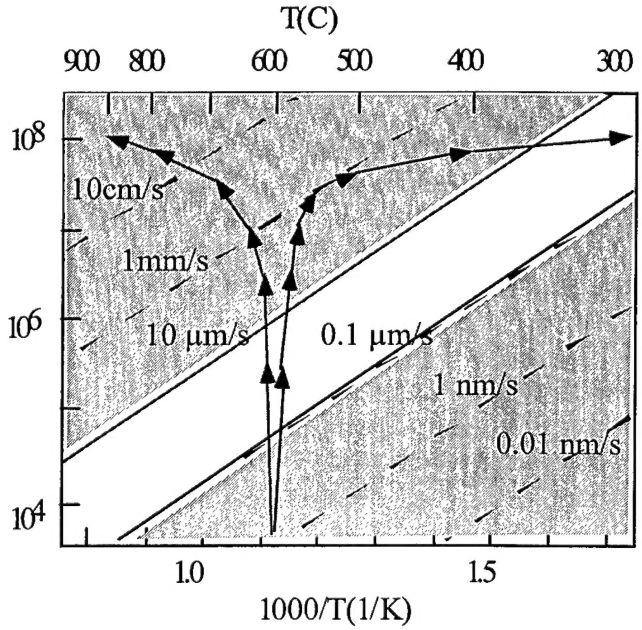


Figure 2. Graph showing the dislocation velocity during the growth of GaAs on Si. The red curve (left) shows the speed of dislocation under compressive stress during annealing. When the curve moves into the upper left (red) shaded region, dislocations are confined effectively. During sample cooling, the sign of the stress in GaAs is reversed so the confined dislocations tend to be unleashed. The right (blue) curve shows the speed of the dislocations under the tensile stress. When the curve goes outside the lower right (blue) shaded region, dislocations obtain enough speed to thread up again. The number on each parallel line indicates the speed of dislocations at given stress and temperature.

Using the information in Figure 1 and the thermal and elastic properties of the substrates and epitaxial layers, we generate a graph that shows how threading dislocations can be confined or be unleashed during the entire growth/annealing/cooling process. Figure 2 shows the result for the classical case of heteroepitaxial GaAs-on-Si growth.

Because GaAs and Si have large thermal mismatch, large thermal stress exists during the heating and cooling cycles. Although the large compressive stress during annealing helps confine the dislocations, the large tensile stress during sample cooling quickly unleash dislocations, to a large extent, canceling the benefits from annealing. In Fig. 2 the red curve (left) shows the speed of dislocation increases under compressive stress during annealing from 600C (growth temperature) to 900C. When the curve moves into the upper left (red) shaded region, dislocations are confined effectively because of their very high speed of movement. During sample cooling, the sign of the stress in GaAs is reversed so the confined dislocations tend to be unleashed. The right (blue) curve shows the speed of the dislocations under the tensile stress. When the curve goes outside the lower right (blue) shaded region, dislocations obtain enough speed to thread up to become threading dislocations again, thus degrading the film quality. Our theory agrees well with the published experimental results (Fig. 3) [1].

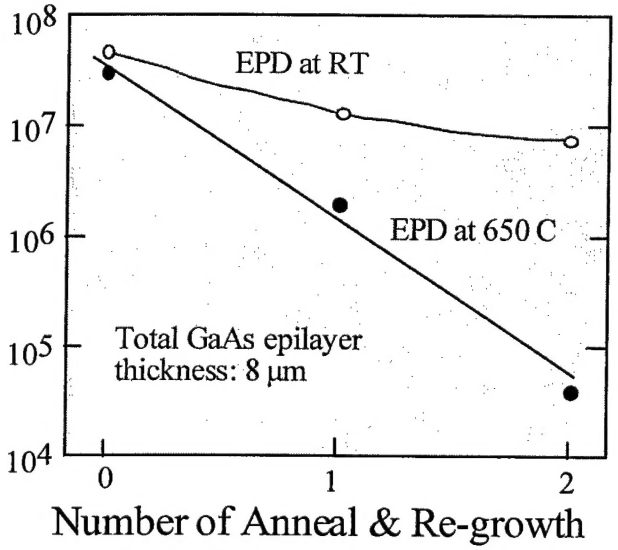


Figure 3. Etch-pit-density for GaAs-on-Si measured at growth temperature (lower blue curve) and at room temperature (upper red curve). (from Tchikawa and Mori, Appl. Phys. Lett., 56 (22), 1990)

Without cooling, the in-situ etch-pit density measurement in GaAs shows a drastic reduction in threading dislocation density at a much faster rate than predicted by the 1/h law. However, when the sample is cooled to room temperature, the obtained improvement largely disappears. This is exactly what has been predicted by our model in Fig. 2. To overcome the above problem, we fabricated a stress-engineered substrate illustrated in Fig. 4.

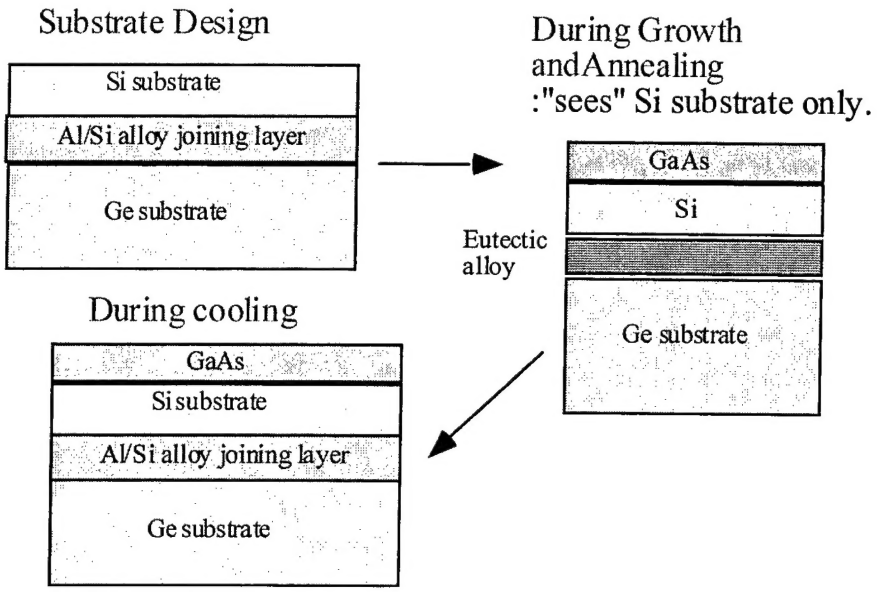


Figure 4. Schematic of the stress-engineered Si substrate for GaAs growth. The thermal stress is regulated by the Al/Si joining layer and the Ge bottom substrate.

The stress-engineered substrate consists of a relatively thin (40 to 50 μm) Si substrate, a very thin (about 1 μm) sputtered Al/Si joining layer, and a thick (350 μm) Ge substrate. An improved wafer bonding process enables us to form such substrate structure without cracking or large voids. At the growth and annealing temperature, the joining layer forms eutectic alloy with Ge and Si and behaves as liquid. This essentially separates the bottom Ge substrate from the top Si so the GaAs layer is stressed as if it is grown on a bulk Si substrate. During cooling, the joining layer is significantly hardened and the bottom Ge contributes significantly to the effective thermal expansion coefficient of the overall substrate. Since Ge is thermally matched to GaAs and the Al/Si/Ge alloy has a larger thermal expansion coefficient than GaAs to counter balance the thermal mismatch between GaAs and Si, the GaAs film will have little stress during cooling. The detailed calculation is shown in Fig. 5.

Because of substrate stress engineering, enough stress for dislocation confinement is achieved during annealing but the stress during cooling is reduced significantly to keep the right branch of the curve within the lower right shaded area. As a result, the confined dislocations will not be unleashed during cooling. The above Si/Al/Ge substrate or other substrate structures may also be used for growth of InP on Si based on the same principle. However, it is important to calculate the dislocation velocity graph as in Figs. 3 and 5 for each new epitaxial material and substrate design to make sure the left and right branch of the curve falls in the desired areas respectively. Figure 6 shows the preliminary results of InP growth on GaA surface. The GaAs "template" is in fact a layer grown on a stress-engineered Si/Ge substrate. Because of the limit in annealing temperature for InP and the modest amount of stress in InP, the effect of dislocation confinement is less pronounced compared to GaAs-on-Si growth. Nonetheless, the improved material quality demonstrates the key concept of substrate stress-engineering.

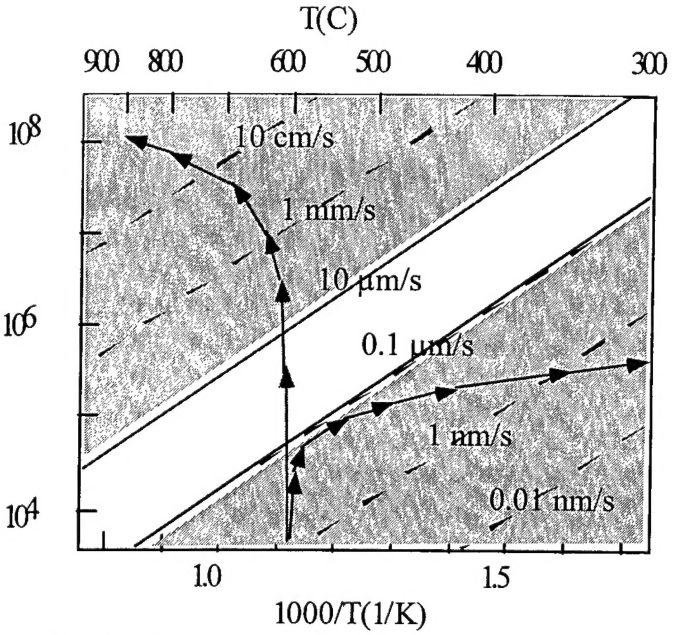


Figure 5. Dislocation velocity during annealing (left red curve) and cooling (right blue curve) for GaAs layers grown on a stress-engineered substrate.

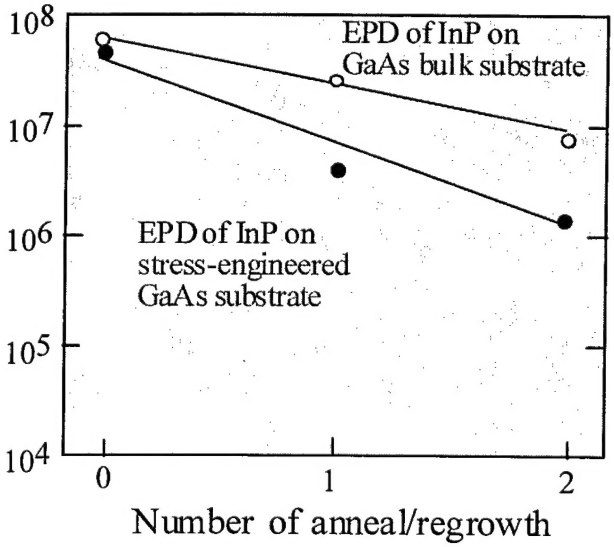
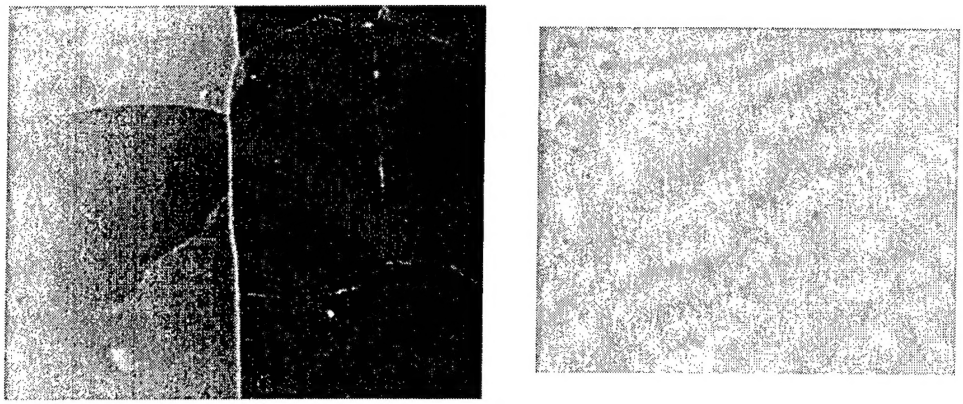


Figure 6. Etch pit density for InP growth on GaAs bulk substrate and Si/Ge stress-engineered substrate with a GaAs buffer layer.

Besides the optimization of substrate design and epitaxial growth, the most important issue from a practical point of view is the fabrication technology for stress-engineered substrate. The technical challenge in substrate fabrication is tremendous due to the fact that the bonded substrate made of thermal mismatched materials has to sustain a wide range of temperature. The substrate has to go through temperature cycles of hundreds of degrees from below room temperature to the highest annealing temperature needed for dislocation confinement. The large built-in stress in the substrate itself often causes wafer cracking and/or debonding. Figure 7 shows the optical micrographs of the bonded Si/Al/Ge stress-engineered substrates using

different bonding methods. With process improvement, we have successfully demonstrated 2" stress-engineered wafers without cracking after going through 20C to 700C thermal cycles. Work is going on to extend the temperature range to 900C.



(a) (b)

Figure 7. Si/Al/Ge stress-engineered substrate using (a) conventional and (b) our improved bonding process.

Wafer warping is another important concern for stress-engineered substrates. To avoid wafer warping and built-in stress within the substrate itself, we prefer stress-free room temperature wafer bonding. However, this often means that the bonded substrate has to sustain the largest temperature variation during growth and annealing. On the other hand, if the substrate is synthesized at a higher temperature, the temperature variation the substrate has to go through can be reduced, at the expense of sample warping and built-in stress at room temperature. The warpage problem becomes more serious with the increasing wafer size. One would be dividing the substrate into smaller (e.g. 1 cm^2) areas. As long as the size of each isolated area is much greater than the substrate thickness, the effect of dislocation confinement will not be affected.

Wafer scale substrate process and device demonstrations

The concept and technique of stress-engineered substrate may find broad applications in electronic and photonic devices. Following is a list of a few important applications of the technology.

I. Semiconductor lasers (particularly surface-emitting lasers) of different wavelengths (visible to IR) on different substrates.
II. Photodetectors of wider operating spectral range.
III. Tensile stressed Si MOSFETs on high-quality, relaxed SiGe templates.
IV. High efficiency solar cells.
V. High brightness light emitting diodes (LEDs) on transparent substrates.
VI. Optoelectronic integrated circuits.
VII. High power/efficiency RF and high speed circuits.

To summarize, the applications of stress-engineered substrates may be divided in two categories. In the first category, the substrate technology allows the formation of semiconductor devices of unique properties including reach of new spectral range and achievement of superior

performance. In the second category, the substrate technology allows integration of devices and circuits made of otherwise incompatible semiconductor materials. The realization of either type of applications will lead to major advance in microelectronics and optoelectronics. Various device applications using the innovative substrate and wafer bodning technologies have been demonstrated by the PI's groups and others.

Besides the quality of the material, another important issue is the scalability of the technology. In the past, we made all the proof-of-concept demonstrations on small wafer pieces (about 1x1 cm^2). Scalability of the technology to full size wafers has always been a key concern in our interactions with industry. Scaling the substrate process to large size wafers involves technological issues such as wafer cleaning, handling, cleanness of the environment, and the instrument/fixture design. Today all these technological issues have been addressed effectively after a substantial investment in equipment and manpower were made. A more fundamental issue for scalability of the process is the stress dependence on the size and geometry of the wafers. In this program, we developed a deep understanding of materials response to different stress fields at different temperatures, thus providing the insight for the process design. We have developed knowledge how microcracks, peeling, and dislocation nucleation, pinning, and multiplication may react to the stress fields in different materials at different temperatures. With the better understanding of the physics and improved processing technology, we have been able to fabricate 2 to 4 " wafers with less than 10 to 50 defect counts.

Figure 8 shows the well-known curve about how the bonding strength of Si-Si varies with the annealing temperature. We have found that the characteristics of III-V to Si and SiGe to Si bonding follow approximately the same characteristics. The curve suggests that two activation energies exist due to the microscopic characteristics of bonding mechanisms. To obtain good bonding strength for reliable and robust material, one needs to bond the materials at high enough temperature. However, one key finding we made in our investigation was that, in order to scale the process to a full wafer process and to reduce the defect counts, one has to use a 2-step annealing process, adding a low T annealing step before raising the temperatures to >300C. The low temperature step is for surface outgasing and is particularly critical to compound semiconductors. Figure 9 shows the experiment to support our statement. We bonded a III-V thin film (1 μm thick) to a Si substrates with different sizes of circular trenches. After bonding, the circular trenches became closed cavities, as shown schematically in the inset of Figure 9. We heated the van der waal bonded structure at different temperatures and then observed the wafer under optical microscope after the bonded structure was cooled to room temperature. When the bonding temperature was below certain range, no appreciable morphological difference could be observed. However, once the bonding temperature reached a threshold value, all cavities became convex at room temperature, indicating that significant surface outgasing occurred at a certain temperature. From the curvature and size of the cavity and the mechanical property of the material, we can calculate the amount of surface outgas in number of atoms per centimeter square. Without going into much detail, the significance of the experiment was to confirm the importance of setting the right temperature cycles for different material systems in order to form high quality, large area bonded substrates or device structures. Otherwise, one will always suffer from high substrate/structure defects although devices of satisfactory performance could be obtained in some "good" areas.

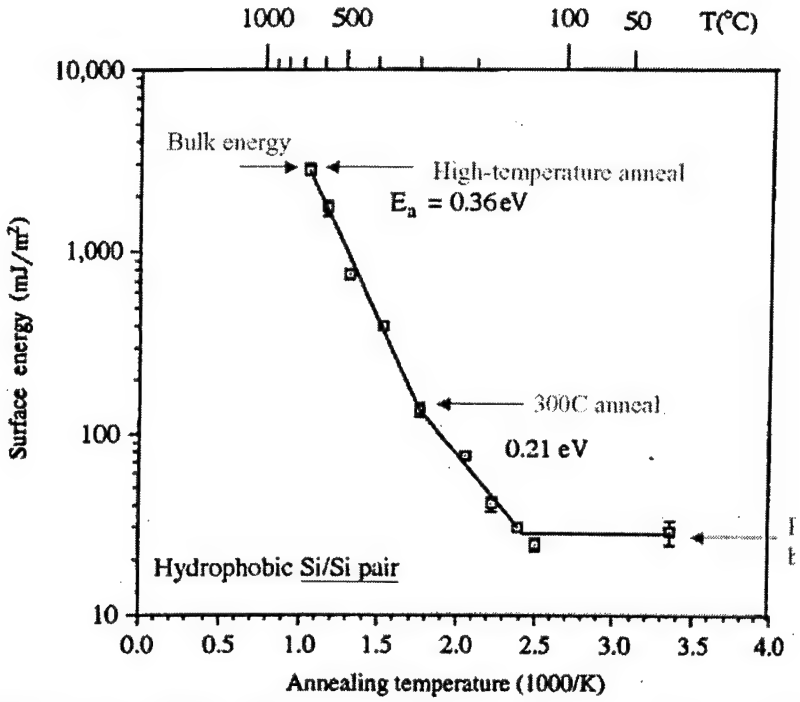


Figure 8. Dependence of surface energy on annealing temperature for bonded Si substrates. Two activation energies can be identified due to the change of bonding mechanisms.

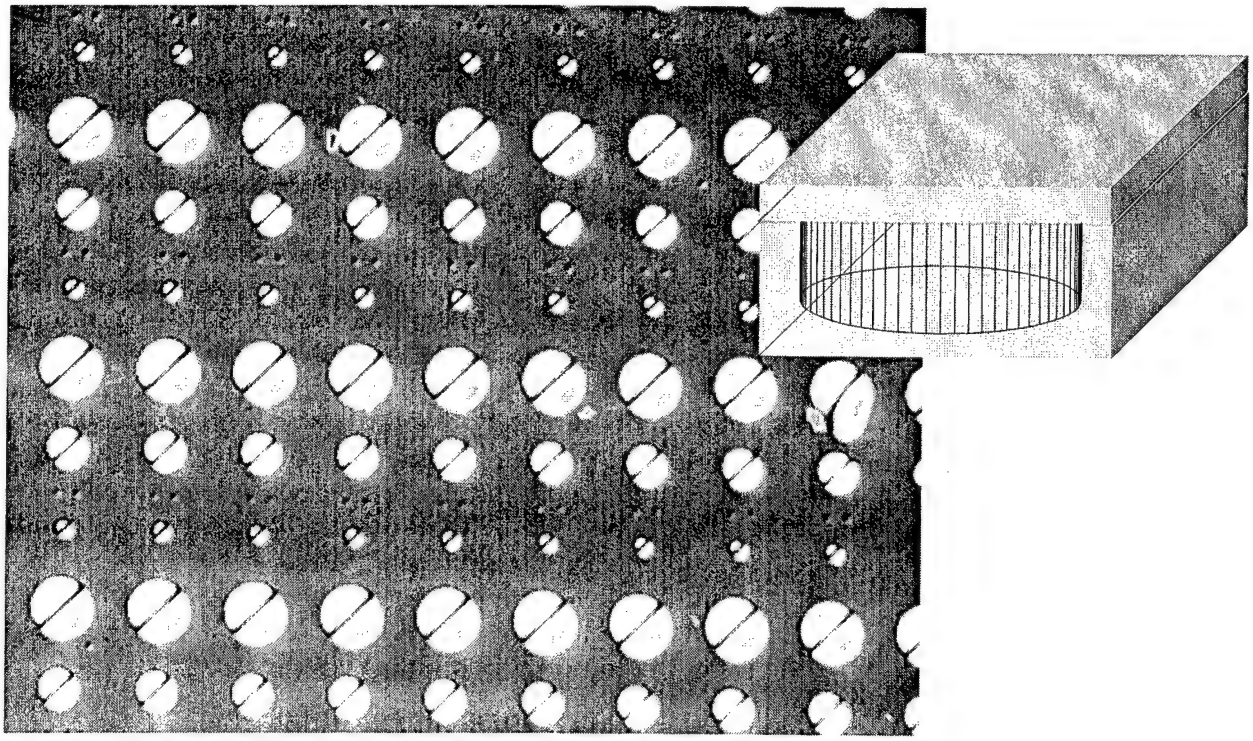


Figure 9. An optical microscope photograph showing the effect of surface outgasing during bonding.

Although the device work is outside the scope of this program, we would like to summarize some key material aspects of these results. Figure 10 shows the SEM photograph of an array of 850nm vertical-cavity surface-emitting lasers (VCSELs) on Si substrates. The VCSELs had a lowest threshold current of 620 μA and a slope efficiency as high as 40%. A larger area device shows a maximum output power of 20 mW and a single spatial mode output of 7mW. All these device results are comparable to the state-of-the-art commercial VCSEL products formed on native GaAs substrates. This is the first demonstration that high performance VCSELs can be made on Si substrates, paving the way to intrachip optical interconnect. Two approaches were performed to create such devices. The first approach is to create a GaAs/Si substrate platform and then grow the VCSEL epitaxial layers on the new substrates. The second approach is to grow the entire GaAs VCSEL epitaxial layers and then transfer them to a Si substrates. In either approach, the bonding between GaAs and Si interface is covalent and free of any joining materials. This is considered as a more attractive approach than hybrid integration using solder bumps or flip-chip bonding. Although we did not really use stress-engineered Si substrates to make VCSELs on Si, the knowledge and technology for stress engineering have been critical to the success of the device demonstration. Since the GaAs VCSEL structure contains as thick as 6 μm epitaxial layer, the GaAs layers would have been shattered or cracked by thermal stress due to the large thermal mismatch between GaAs and Si without the knowhow of stress engineering developed in this program.

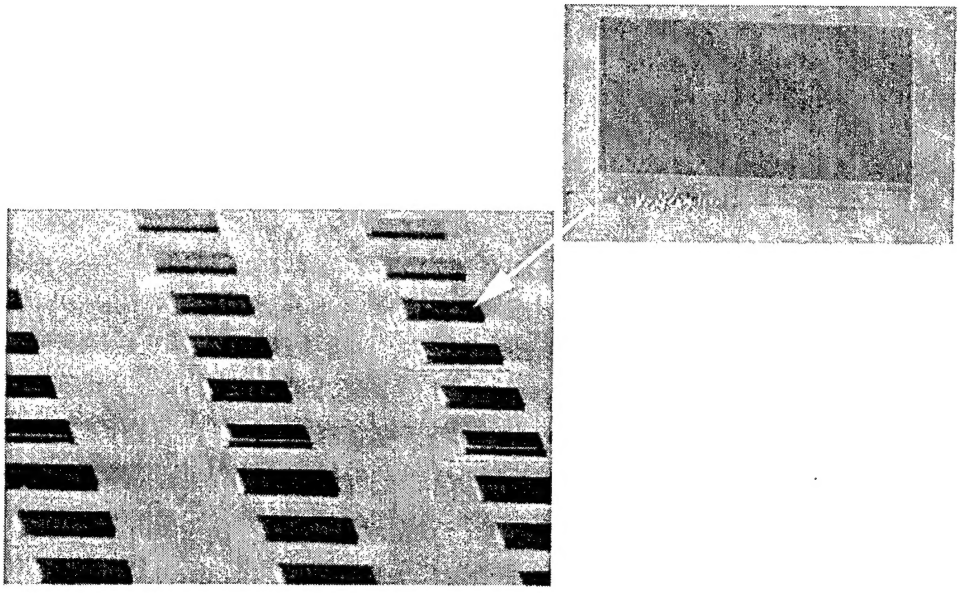


Figure 10. SEM photograph of a 2-D array of GaAs VCSELs on Si substrates using wafer bonding and stress-engineering techniques.

In another example, we adopted the stress control technique to create InP/InGaAs/Si heterostructure avalanche photodetectors (APDs) with superb characteristics. Avalanche photodetectors produced about 10 times better sensitivity than PIN photodetectors and therefore are attractive choices for high-end photoreceivers. The key issue for the currently all III-V APDs is the high excess noise due to the InP multiplication region. If this multiplication region can be made of Si, significant noise reduction can be obtained due to the more favorable material properties. Our wafer engineering technology offers opportunities to form such structures. As

shown in Figure 11, excellent heterointerface between InP and Si can be obtained. Such high quality interface supports electron transport from InGaAs to Si and hole transport in the reverse direction. Without the stress engineering technique, there will be many dislocations in an extended region to cause filamentation (nonuniform or early breakdown), high leakage current, and high 1/f noise. In collaboration with Nova Crystals, which licensed three patents on substrate technologies from Cornell University in 1998, we have demonstrated the InGaAs/Si APDs with a world record low excess noise (F = 2.6 at a multiplication factor of 50). The measured noise approaches the quantum limit of F = 2, manifesting the high quality of the heterointerface and the effectiveness of the stress engineering concept and technology. Figure 12 shows an optical microscope photograph of a processed InGaAs/InP/Si wafer. Under careful inspection, no visually identifiable defects were observed under microscope over about 1,000 devices occupying an area of 1x1 cm^2. This result shows that the density of microscope detectable wafer defects is less than one per centimeter square, or a single digit defect count for a whole 2" wafer.

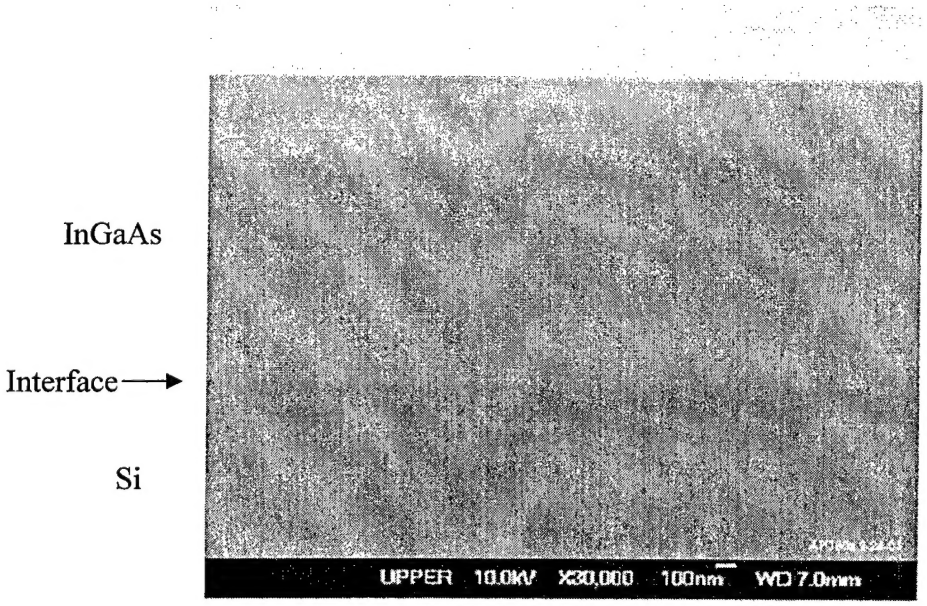


Figure 11. SEM photograph of the cross section of an InGaAs/Si avalanche photodetector (APD).

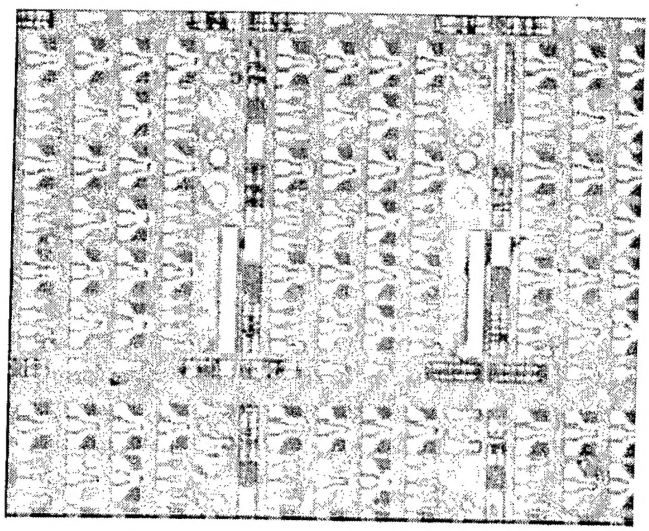


Figure 12. Microscope photograph of InGaAs/Si APDs fabricated on a Si substrate. After all the thermal and chemical processes, no material defects were observed under optical microscope.

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